Impact of Contact on the Operation and Performance of Back-Gated Monolayer MoS_2 Field-Effect-Transistors

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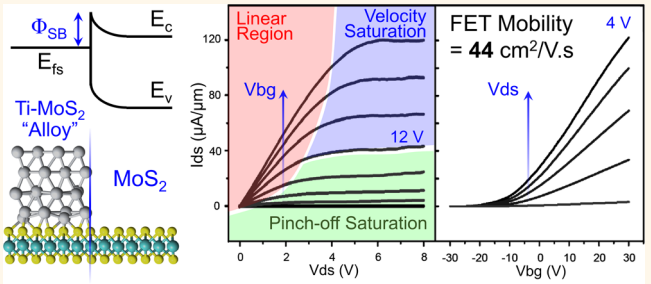
ABSTRACT Metal contacts to atomically thin two-dimensional (2D) crystal based FETs play a decisive role in determining their operation and performance. However, the effects of contacts on the switching behavior, field-effect mobility, and current saturation of monolayer MoS_2 FETs have not been well explored and, hence, is the focus of this work. The dependence of contact resistance on the drain current is revealed by four-terminal-measurements. Without high-κ dielectric boosting, an electron mobility of 44 $cm^2/(V \cdot s)$ has been achieved in a monolayer MoS_2 FET on SiO_2 substrate at room temperature. Velocity saturation is identified as the main mechanism responsible for the current saturation in back-gated monolayer MoS_2 FETs at relatively higher carrier densities. Furthermore, for the first time, electron saturation velocity of monolayer MoS_2 is extracted at high-field condition.



KEYWORDS: 2D semiconductor · contact · current saturation · field-effect transistor · molybdenum disulfide · Schottky barrier · transition metal dichalcogenides

Along with the continuous scaling of devices in the semiconductor industry, it is generally accepted that Si (including ultrathin Silicon-on-Insulator (SOI))-based complementary metal–oxide–semiconductor (CMOS) technology will reach its scaling limit (below 5 nm) due to the bulk nature of silicon.[1] Therefore, new semiconductor materials alternate to silicon should be developed to avoid those scaling issues in Si-based CMOS technology. Monolayer MoS_2, one of the transition-metal dichalcogenides (TMDs), shows great potential for nanoscale (sub-5 nm) FET applications owing to its atomic thickness (0.65 nm), excellent thermal stability, considerable band gap (~1.8 eV), and pristine interfaces (without out-of-plane dangling bonds).[1−4] The atomically thin MoS_2 provides excellent gate electrostatic control to suppress short-channel-effect (SCE),[5,6] which is one of the major issues in nanoscale MOSFETs. In addition, the large effective mass of monolayer MoS_2 can reduce the source/drain direct tunneling, thereby leading to small subthreshold swing (SS). Recently, monolayer MoS_2 FET has been experimentally demonstrated with a small SS of 74 mV/decade, and an ON/OFF ratio of ~10^8, indicating that monolayer MoS_2 is suitable for low-power digital applications.[1−11] However, the interface between 2D semiconductors and three-dimensional (3D) metal contacts is one of the major parameters, which determines the performance of all 2D material based nanoelectronic devices.[11−15] This has been proved in several reported MoS_2 works,[15,16] in which contact resistances at the metal/MoS_2 interfaces significantly limit the device performances.

Fermi level pinning is a common issue in low dimensional materials with metal contacts. It has been proved that there is severe Fermi level pinning between MoS_2 and metal.[17] Hence, Schottky barrier always exists between monolayer MoS_2 and contact metals. Although small Schottky barriers (30 meV with Sc and 50 meV with Ti) have been achieved between few-layer or multilayer MoS_2 and contact metals,[18] such small Schottky barriers still influence the device operation.[19] Compared with multilayer MoS_2, monolayer MoS_2 has smaller electron affinity (4.2 eV). Therefore, according to

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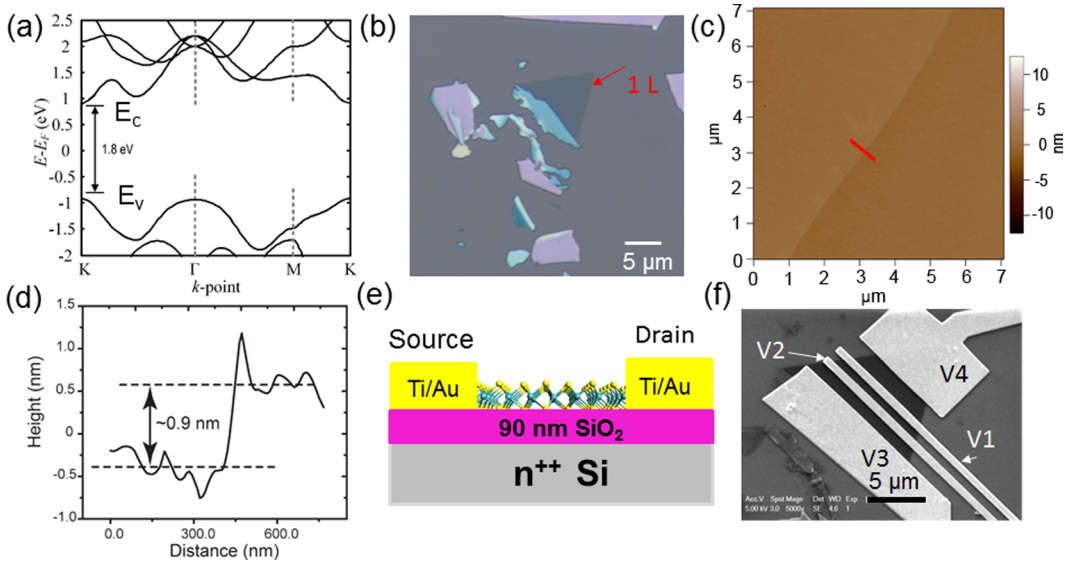

Figure 1. (a) Energy dispersion of monolayer MoS_2. Monolayer MoS_2 has a direct band gap of 1.8 eV. (b) Optical microscope image of monolayer MoS_2 on SiO_2 (90 nm)/Si. (c) AFM image and (d) height profile of monolayer MoS_2. The height profile is measured along the red line in (c). (e) Schematic view of the back-gated monolayer MoS_2 FET. (f) SEM image of the fabricated back-gated monolayer MoS_2 FET. In four-terminal-measurements, current flows (I_{ds}) from V4 to V3. The voltages are measured on V1 and V2. Channel resistance is calculated as (V1 − V2)/I_{ds}. The details of resistance extraction is shown in Supporting Information S2.

the Schottky theory, the Schottky barrier between monolayer MoS_2 and Ti (work function = 4.33 eV) should be larger, thereby affecting the device performance to a greater extent. However, ambiguities still exist in the understanding of the nature and impact of such contacts on the characteristics and operation of monolayer MoS_2 FETs, such as switching behavior, current saturation and field-effect mobility.

Various metals such as Ti, Au, Ni, Mo, and Sc have been used as the contact metal with monolayer or multilayer MoS_2.[2,5−19] Recent theoretical and experimental works have shown that titanium (Ti) can form a good contact with monolayer MoS_2 (monolayer MoS_2 has a direct band gap of 1.8 eV (Figure 1a)),[11,12] in which Ti shows high capability to dope MoS_2 (under the contact region). Since Ti shows promise as a contact metal with MoS_2, we select Ti as the contact metal to study the impact of contacts on the operation and performance of monolayer MoS_2 FETs. On the other hand, we observed a current degradation after depositing 30 nm HfO_2 dielectric film on top of monolayer MoS_2 (Supporting Information S1). Hence we choose back-gated FET configuration to study the metal contact to MoS_2 and intrinsic mobility of MoS_2 in this work.

Monolayer films are prepared by mechanical exfoliation of bulk MoS_2 (SPI Instrument, Inc.) onto 90 nm SiO_2/Si (highly *n*-doped) substrate. The thickness of MoS_2 film is identified using optical microscope (Figure 1b) since we have established the correlation between optical contrast of monolayer TMD and thickness of underlying dielectric.[19] The thickness of monolayer MoS_2 is further confirmed by AFM (Figure 1c,d). The measured thickness of monolayer is around 0.9 nm due to the absorbed molecules on top of MoS_2. Heavily *n*-doped Si is used as the back gate as shown in Figure 1e. The SEM image of the fabricated back-gated FET device is shown in Figure 1f. After metal lift-off, device is loaded into Lakeshore vacuum probe station. All measurements are performed in vacuum (1×10^{-6} mbar) at room temperature after annealing in the vacuum (3×10^{-6} mbar) at 420 K for 12 h to remove any absorbed moisture and solvent molecules.

RESULTS AND DISCUSSION

In a metal contact with MoS_2 as shown in Figure 2a, there are two components contributing to the contact resistance, which are the tunneling barrier between metal and MoS_2 below the contact metal due to the van der Waals (vdW) gap (dash line A in Figure 2a), and Schottky barrier between contact and channel (dash line B in Figure 2a). In this work, density functional theory (DFT) calculation is employed to explore the electronic nature of the contact between Ti and monolayer MoS_2. The details of the setup used for DFT calculations are included in the Supporting Information S3.

Electronic dispersion of MoS_2 with Ti is studied to estimate the Schottky barrier between monolayer MoS_2 and Ti by DFT as shown in Figure 2c. In Figure 2c, the red lines indicate the bands of monolayer MoS_2 with a band gap of 1.8 eV. Gray lines show the bands of Ti−MoS_2 system, indicating that the original MoS_2 bands (red) are completely disturbed by the Ti atoms due to strong hybridization between Ti and S orbitals. The new bands (gray) of the Ti−MoS_2 system display a metallic behavior with a zero band gap, implying that MoS_2 under Ti area is completely metallized by the hybridization between Ti and S atoms. This metallization is also confirmed by the PDOS of the

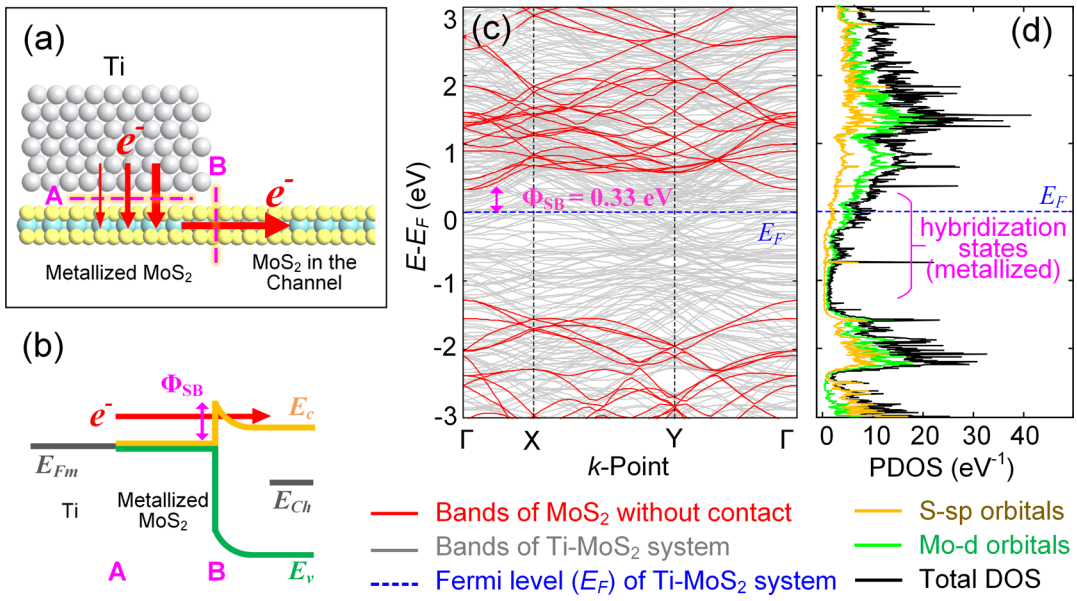

Figure 2. (a) Schematic of electron injection direction in MoS_2 and contact metal: A, tunneling barrier between metal and MoS_2 below contact metal; B, Schottky barrier between contact and channel. (b) Band diagram illustrating the Ti−MoS_2 Schottky barrier. (c) Electronic dispersion of MoS_2 without contact (red lines) and with Ti contact (grey lines). (d) PDOS of sp orbital of S atoms (yellow line) and d orbital of Mo atoms (green line).

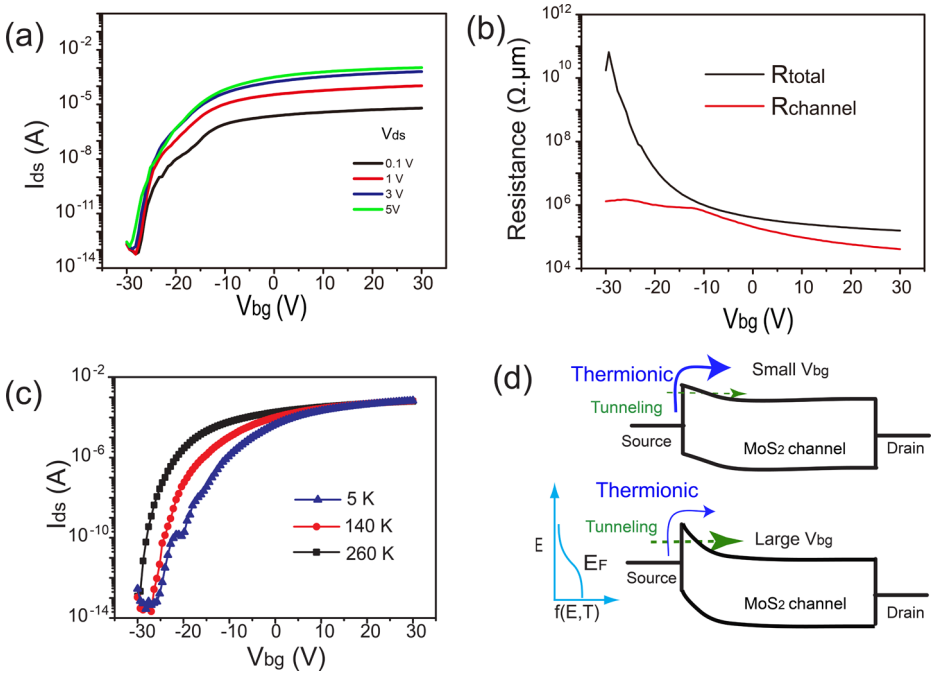

Figure 3. (a) I_{ds}−V_{bg} curve of monolayer MoS_2 back-gated FET with Ti contact. (b) Channel resistance ($R_{channel}$), and total source-drain resistance (R_{total}) as a function of back-gate voltage (V_{bg}). (c) Temperature dependent I_{ds}−V_{bg} curves of back-gated monolayer MoS_2 FET with Ti contact, V_{ds} = 3 V. (d) Band diagram of MoS_2 back-gated FET with Ti contact at different V_{bg}.

Ti−MoS_2 system (Figure 2d). As shown in Figure 2d, the original band gap of MoS_2 vanishes after contacting with Ti. Hence, the tunneling barrier height is zero between Ti and MoS_2 due to the metallic behavior of Ti−MoS_2 system. Therefore, contact resistance is solely contributed by the Schottky barrier between the contact area (Ti−MoS_2 system) and the monolayer channel MoS_2 (Figure 2b). By comparing the band structure of MoS_2 (bottom of conduction band) with the Fermi level of Ti−MoS_2 system (given by DFT, Figure 2c), a 0.33 eV Schottky barrier can be extracted. This Schottky barrier (0.33 eV) is consistent with our experimental measurements that yielded 0.3−0.35 eV, which is shown in the next section.

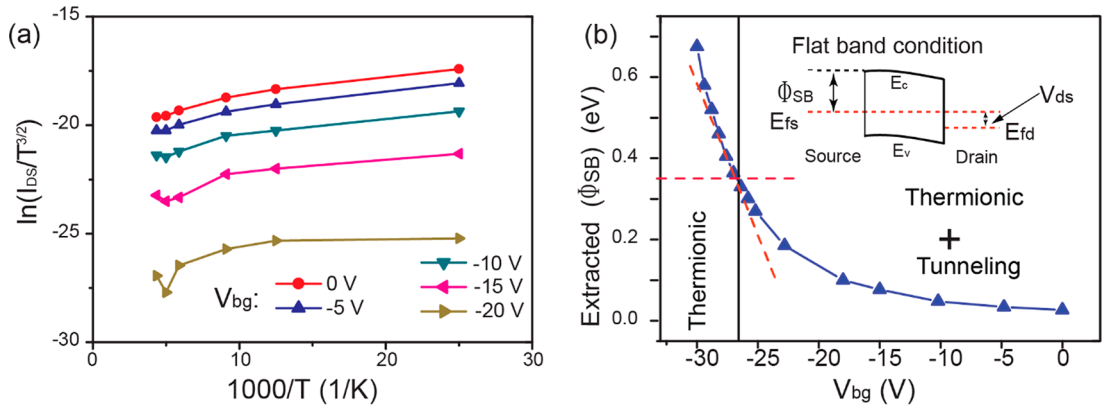

Figure 4. (a) Arrhenius-type plot of ln ($I_{ds}/T^{3/2}$) *vs* 1000/*T* at different V_{bg}. (b) Extracted effective barrier height (Φ_{SB}) as a function of V_{bg} for monolayer MoS_2 FET with Ti contact. Inset shows the band diagram at flat band condition.

Figure 3a shows the transfer characteristics of the back-gated monolayer MoS_2 FET with Ti (10 nm)/Au (100 nm) contact. It clearly displays an *n*-type behavior with ON/OFF ratios (defined as the ratio of maximum to minimum drive current in the V_{bg} range of −30 to 30 V) exceeding 10^6 at V_{ds} varying from 0.1 to 5 V. Four-terminal-measurements are employed to measure the $R_{channel}$ as denoted by the red curve in Figure 3b. Black curve in Figure 3b corresponds to the R_{total} ($R_{total} = 2R_c + R_{channel} = V_{ds}/I_{ds}$) measured by two-terminal measurements (between V1 and V2 in Figure 1f) at $V_{ds} = 0.1$ V. R_{total} shows a large variation, which is $\sim 10^6$ for V_{bg} swept from −30 to 30 V. Hence, for back-gated monolayer MoS_2 FET with Ti contact, the switching mainly occurs due to modulating the contact.

To clearly understand the mechanism of current injection in monolayer MoS_2 FET with Ti contact, temperature dependent measurements are performed. Figure 3c shows the temperature dependent $I_{ds}-V_{bg}$ curves of monolayer MoS_2 FET with Ti contact. When the V_{bg} is below 10 V, the source drain current (I_{ds}) clearly shows temperature dependent behavior, indicating that thermionic emission dominates the electron injection at low V_{bg}. At high temperatures, electrons can occupy higher energy levels leading to more electrons flowing over the Schottky barrier and contributing to the current injection. I_{ds} becomes less dependent on the temperature when V_{bg} is above 10 V, implying that tunneling dominates the current at high V_{bg} due to the narrowing of the Schottky barrier, which is created by the band bending near the MoS_2−Ti contact (Figure 3d).[17]

Since the DFT calculation predicts a 0.33 eV Schottky barrier between Ti and monolayer MoS_2, hence, in order to understand the Schottky barrier effect on monolayer MoS_2 FET operation, it is necessary to measure the Schottky barrier between Ti and monolayer MoS_2. The expression of thermionic emission current for 2D material can be derived as $I = A_{2D}WT^{3/2}e^{-(q\Phi_{SB}/K_BT)}(1 - e^{-(qV_{ds}/k_BT)})$, where q is the magnitude of the electron charge, Φ_{SB} is the Schottky barrier height, W is the width of the contact with 2D material, k_B is the Boltzmann constant, and V_{ds} is the drain-source bias. A_{2D} is the Richardson's constant for 2D materials and is derived to be $A_{2D} = \{[2(2\pi)^{1/2}g_v q\sqrt{m^*}]/h^2\}k_B{}^{3/2}$, where g_v is the valley degeneracy, h is Planck's constant, and m^* is in-plane effective mass of monolayer MoS_2. The derivation of thermionic emission current for 2D material is shown in the Supporting Information S4. By comparing the thermionic emission equations of 2D material and bulk material, one can find that temperature dependence is lower for 2D material compared to that of 3D material. In addition, the Richardson's constant is also different for 2D material and 3D material (with different units).[20]

Figure 4a shows the Arrhenius plot for various gate voltages, which is measured by two-probe measurement. The slope of the Arrhenius plot (Figure 4a) can be used to analyze the Schottky barrier from the thermionic emission theory. Schottky barrier height as a function of V_{bg} is shown in Figure 4b. As mentioned in ref 18, it is necessary to evaluate the flat-band gate voltage because it is a benchmark to identify the transition point between the tunneling current and the thermionic emission current. When the gate voltage is below the flat-band gate voltage, the thermionic emission predominantly contributes to the current. Hence, using the thermionic emission equation for 2D materials, the Schottky barrier between MoS_2 and Ti can be accurately extracted. The extracted Schottky barrier between monolayer MoS_2 and Ti varies from 0.3 to 0.35 eV measured from six different monolayer devices. The Schottky barrier between monolayer MoS_2 and Ti is significantly larger than the Schottky barrier between multilayer MoS_2 (bandgap: 1.2 eV) and Ti, which is around 50 meV.[18] The extracted Schottky barrier between monolayer MoS_2 and Ti is quite reasonable given that monolayer MoS_2 has smaller electron affinity than multilayer MoS_2. The value of the Schottky barrier height is also consistent with the DFT calculation, which confirms the accuracy of our contact model.

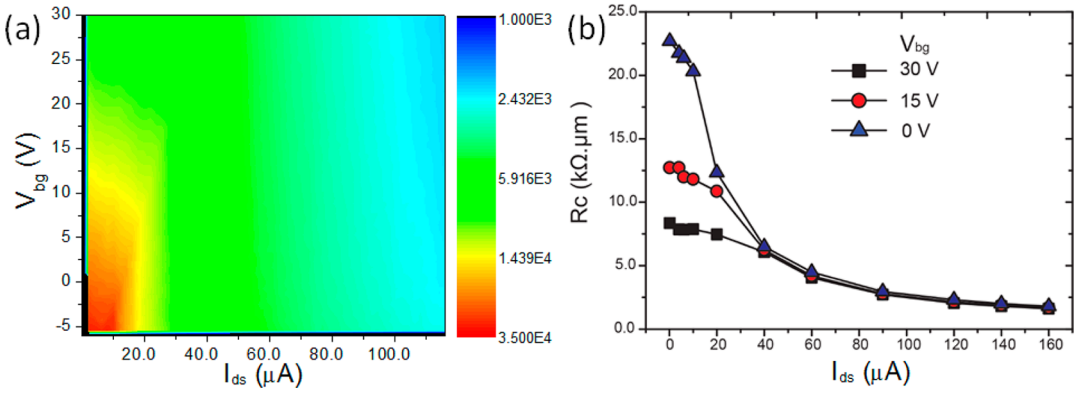

Figure 5. (a) Contour plot of R_c ($\Omega \cdot \mu$m) as a function of V_{bg} and I_{ds} used for the 4-point measurements. (b) R_c as a function of I_{ds} at various V_{bg}.

As mentioned above, MoS_2 FET with Ti contact has a large Schottky barrier. To study the effect of contact on the performance of MoS_2 FET, it is desirable to extract the contact resistance. Four-terminal-measurement method is employed to extract the contact resistance (R_c) at various V_{bg}. By injecting a constant current (I_{ds}) into the four-terminal configuration (between V4 and V3 in Figure 1f), $R_{channel}$ (between the inner two electrodes, V1 and V2, as shown in Figure 1f) can be directly measured. Then, R_{total} (R_{total} = (V1 − V2)/I_{ds}) between V1 and V2 is measured using two-terminal-measurements by applying the same current employed in the four-terminal-measurements. Hence, R_c can be extracted by subtracting the $R_{channel}$ from R_{total}.

Figure 5a shows the contour plot of R_c as a function of V_{bg} and I_{ds} applied for the four-terminal-measurements. It is found that R_c is dependent on the values of applied I_{ds} as well as the V_{bg} as shown in Figure 5a. At small I_{ds} (below 20 μA), R_c shows strong V_{bg} dependence, in which R_c is ~25 k$\Omega \cdot \mu$m at V_{bg} = −5 V, while R_c can be reduced to 7 k$\Omega \cdot \mu$m at high V_{bg} (30 V). When I_{ds} > 40 μA, R_c is significantly reduced at low V_{bg} and shows less V_{bg} dependence.

Various R_c's as a function of I_{ds} at V_{bg} = 0, 15, and 30 V are also plotted in Figure 5b. At low I_{ds} (<40 μA), R_c shows distinct V_{bg} dependence, implying that Schottky barrier is mainly tuned by the gate electrostatics. However, when I_{ds} > 40 μA, R_c has less dependence on the V_{bg}, indicating that the amount of electrons injected from source is much larger than the electrons generated by gate electrostatics. Hence, the large amount of electrons injected from source can heavily dope monolayer MoS_2 resulting in a very narrow Schottky barrier. The minimum extracted R_c is ~1.3 k$\Omega \cdot \mu$m (I_{ds} = 150 μA, V_{bg} = 30 V), which is much smaller than any reported value on metal contact with monolayer MoS_2.

Current saturation of MoS_2 FET is important for digital circuit applications (shown in Supporting Information S5), in which it can significantly influence the noise margins.[4] The saturation performance, which can be described by output resistance, determines sharpness of the voltage-transfer curve of a CMOS inverter, and thus the maximum noise margin. Although the atomic scale thickness of monolayer MoS_2 provides excellent electrostatics, current saturation in monolayer MoS_2 back-gated FETs has been rarely observed at low V_{ds}.[21] As mentioned in our previous work, due to the high parasitic series source/drain contact resistance,[15,19] the effective V_{gs} and V_{ds} are lowered and are given by $V_{gs\_eff} = V_{gs} - (R_c \times I_{ds})$ and $V_{ds\_eff} = V_{ds} - (2R_c \times I_{ds})$. R_c can be directly extracted from Figure 5a at given V_{bg} and I_{ds}. This provides the possibility to study the performance of the MoS_2 FET.

Figure 6a−c shows the output characteristics of monolayer MoS_2 FETs with a channel length of 0.8, 1.1, and 1.5 μm, respectively. All of the three I_{ds}−V_{ds} curves display a nearly linear behavior at low V_{ds}, indicating that the Schottky barrier is very narrow. The lowest R_c of our device is ~1.3 k$\Omega \cdot \mu$m with Ti contact at V_{bg} = 30 V. Due to this small R_c, ON-current of our monolayer MoS_2 FET is ~50 μm/μA at V_{bg} = 30 V and V_{ds} = 2V (or 200 μA/μm at V_{bg} = 30 V and V_{ds} = 8 V) which is much higher than any reported values in back-gated monolayer MoS_2 FETs. With a small R_c, robust current saturation can be observed in Figure 6a. However, along with the increase of the channel length, current saturation degrades at high V_{bg} for long channel devices (Figure 6b,c), implying the absence of "pinch-off".

In Figure 6a−c, monolayer MoS_2 FETs have a pinch-off like current saturation when V_{bg} <12 V, in which I_{ds} increases along with increase of V_{ds} until the saturation value is reached. The drain voltages also satisfy pinch-off saturation condition, $V_{ds\_eff} > (V_{gs\_eff} - (R_c \times I_{ds} - V_{th}))/m$. Here, m is the body-effect coefficient that can be derived from subthreshold swing (SS) equation: $SS = 2.3(1 + C_{trap}/C_{ox})mkT/q = 2.3mkT/q$, where C_{trap} is interface trap capacitance, C_{ox} is gate dielectric capacitance, k is Boltzmann's constant, T is temperature and q is electronic charge. The SS of our back-gated FET is around 410 mV/dec. Hence, m is around 7, which

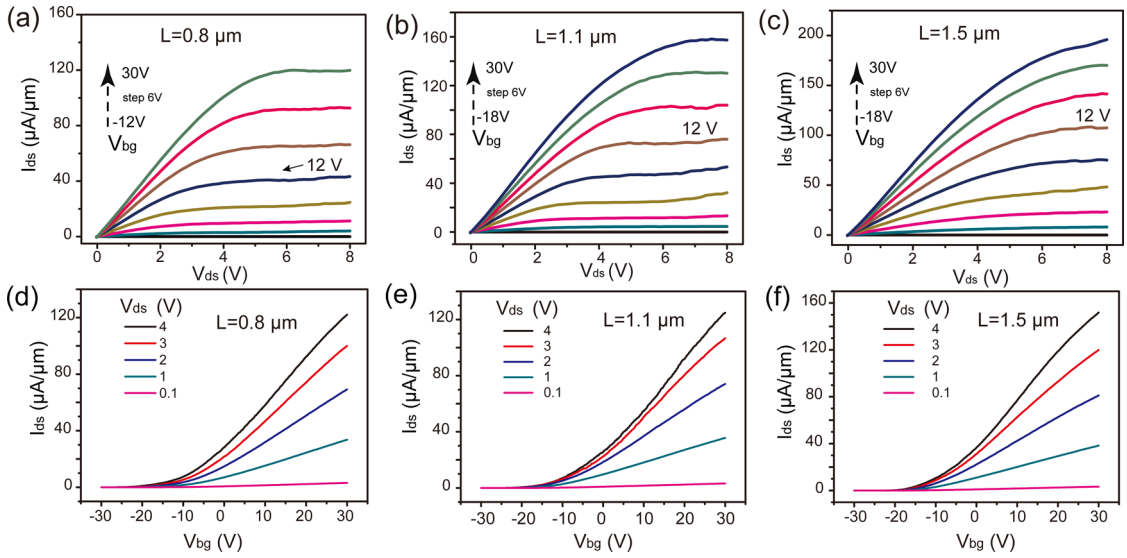

Figure 6. (a–c) Output characteristics of back-gated monolayer MoS_2 FETs. (d–f) Transfer characteristics of back-gated monolayer MoS_2 FETs measured from device (a), (b), and (c), respectively.

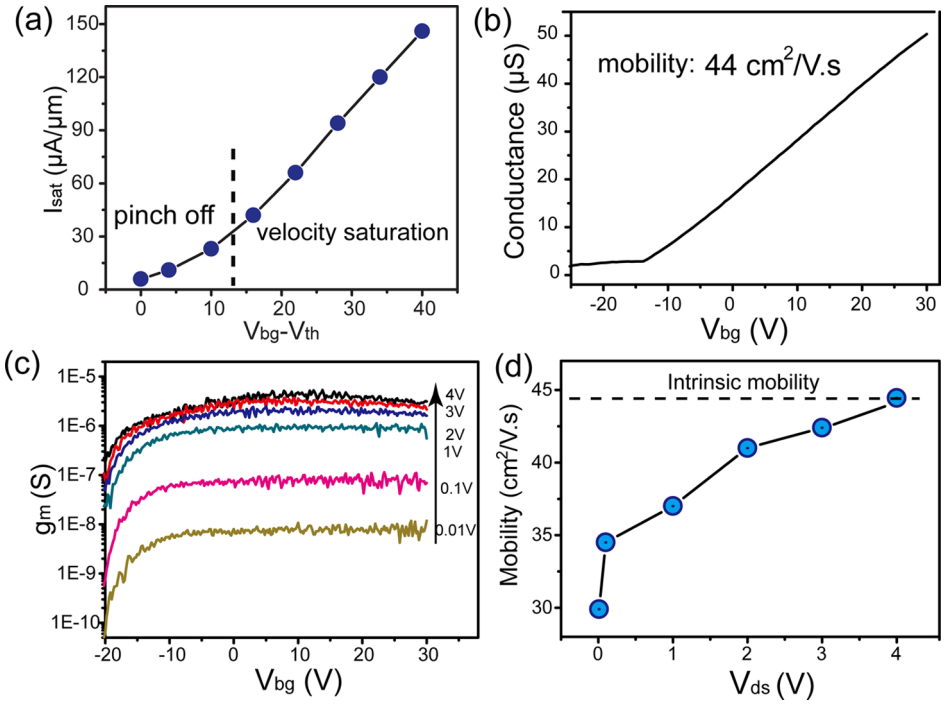

Figure 7. (a) Corresponding I_{sat} as a function of $(V_{bg}-V_{th})$ extracted from device in Figure 6a. (b) Channel conductance (G) of monolayer MoS_2 FET with Ti contact as a function of V_{bg}. Values of G are measured by four-terminal-measurements. $G=1/R_{channel}$. (c) Transconductance (g_m) of monolayer MoS_2 FET as a function of V_{bg} for various V_{ds}. (d) FET mobility (without excluding the effect of contacts) of monolayer MoS_2 as a function of V_{ds}.

indicates a poor gate modulation effect in back-gated FET. The threshold voltage (V_{th}) of our back gated device is approximately −10 V as shown in Figure 6d–f. R_c can roughly be extracted from Figure 5a. In Figure 6a, when V_{bg} = 18 V and I_{sat}= 60 μA/μm (V_{ds} = 4 V, width of the device is 1.5 μm), R_c is ~2.5 k$\Omega\cdot\mu$m. Hence, the ratio between R_c and R_{total} is $\sim 3 \times 10^{-2}$ which indicates that R_c has minimal impact on the ON-current of this device when the channel is fully turned on by the gate.

When V_{bg} < 12 V, I_{ds} increases parabolically along with the increase of V_{ds} until the saturation value is reached. When V_{bg} > 12 V, I_{ds} increases linearly and is proportional to the $(V_{bg}-V_{th})$ as shown in Figure 7a, indicating that device is operated in the velocity saturation region. Four-terminal-measurements also confirm the linear behavior of the conductance as a function of V_{bg} when V_{bg} > 12V (Figure 7b). Hence, the current saturation in monolayer MoS_2 is a

combination of pinch off (at low carrier density) and velocity saturation (at relatively higher carrier density).

For V_{bg} > 12 V and V_{ds} > 4 V, I_{ds} starts to saturate due to velocity saturation. Using equation for current (I_{sat}) under velocity saturation $I_{sat} = WC_{ox}(V_{effec\_bg} - V_{th} - V_{effec\_sat}/2)\upsilon_{sat}$, where W is the width of device, and υ_{sat} is the saturation velocity, the υ_{sat} for monolayer MoS_2 is extracted from Figure 6a to be ~9.85 × 10^5 cm/s at V_{bg} = 30 V and V_{ds} = 6 V, which is close to the theoretically calculated value of ~10^6 cm/s.[22,23]

To improve the drive current for high-performance CMOS applications at ultrascaled dimensions, it is necessary to have high mobility.[24] However, one issue of monolayer MoS_2 is the low mobility, which is in the range of 0.1−13 $cm^2/(V\cdot s)$ on SiO_2 substrate at room temperature.[1,2] In general, the Schottky barrier at the monolayer MoS_2−Ti interface (area B as shown in Figure 2b) introduces a contact resistance that degrades the device performance. Although doping the source/drain area can significantly reduce the contact resistance, currently a reliable technique such as ion implantation to dope the 2D semiconductors without disrupting their desired properties (replacing any atoms destroys the electronic structure of 2D semiconductors) is lacking. Thus, it is necessary to estimate the effect of contact on the extracted FET mobility for the measurements and maximize the performance of monolayer MoS_2 FETs using the gate electrostatic doping that can thin down the tunneling barrier for electron injection. To estimate the effect of contact on the device performance, we first discuss the intrinsic mobility of monolayer MoS_2 flakes on SiO_2 (90 nm)/Si substrate measured in a four-terminal configuration followed by the analysis of effective mobility (including the effect of contact resistance) measured in a two-probe configuration.

The channel conductance (G) of monolayer MoS_2 FET as a function of V_{bg} is measured by four-terminal-measurements. Then, the intrinsic mobility of monolayer MoS_2 can be extracted as $\mu = (L/W)dG/dV_{bg}C_{ox}^{-1}$ in the linear region (Figure 7b), where C_{ox} (3.84 × 10^{-4} $F\cdot m^{-2}$) (the fringing capacitance and quantum capacitance can be ignored for a long channel back-gated FET with thick dielectric film) is the capacitance of the 90 nm-thick bottom SiO_2 dielectric; L and W represent the length and width of the channel, respectively. The mobility of monolayer MoS_2 FET is ~44 $cm^2/(V\cdot s)$ (deducting the effect of contact resistance) at room temperature, which is significantly higher than other reported values (0.1−13 $cm^2/(V\cdot s)$) in literature.[1,2,25,26] This value is also close to the mobility of monolayer MoS_2 after boosting with high-k dielectrics,[5] indicating that there is additional space to further improve the performance of monolayer MoS_2 on SiO_2 substrates. Additionally, as shown in Figure 7b, the conductance is linear over a relatively large range of the back-gate voltage (from −10 to +30 V), indicating that the inherent 2D carrier density remains low. To verify this, the carrier density of monolayer back gated MoS_2 FET is calculated using the method described in ref 4. As shown in the Supporting Information S6, the carrier density of back-gated monolayer MoS_2 FET is linearly dependent on the gate voltage when the gate voltage is greater than the threshold voltage. The calculated carrier density is on the order of ~$10^{13}/cm^2$ (which is considered low) because of the thick dielectric substrate (90 nm SiO_2).

Since the intrinsic mobility of MoS_2 on SiO_2 has been calculated, we can estimate the effect of contact resistance on the mobility extracted through two-terminal measurements. Transconductance (g_m) for various drain voltages are measured through two-terminal measurements as shown in Figure 7c. At high V_{ds}, the changes of g_m tend to saturate. The maximal derived g_m at V_{ds} = 4 V is ~4.8 $\mu S/\mu m$. Then, for two-terminal measurements, mobility can be extracted using the well-known equation: $\mu = (L/W)g_m C_{ox}^{-1} V_{ds}^{-1}$ in the linear region of the $I_{ds}-V_{ds}$ plot without deducting the contact resistance. Figure 7d shows the peak mobility for different V_{ds}. The extracted effective mobility shows a clear V_{ds} dependency (Figure 7d). The extracted effective mobility is around 30 $cm^2/(V\cdot s)$ at V_{ds} = 0.01 V, while the mobility reaches 44 $cm^2/(V\cdot s)$ at V_{ds}= 4 V, which is nearly equal to the intrinsic mobility of monolayer MoS_2 as shown in Figure 7c. This can be attributed to the reduction of Schottky-Barrier width on channel-source side with increase in V_{ds}, indicating that the channel is not efficiently controlled by the back gate with thick gate dielectric. In addition, under high electric field, electrons have high velocity resulting in the reduction of electron localization in MoS_2 system, since electron localization caused by the trapped charges in the SiO_2 substrate are responsible for the low mobility in monolayer MoS_2 FET.[27]

CONCLUSION

In summary, the contact between Ti and MoS_2 dominates the switching of monolayer MoS_2 FETs. Schottky barrier between MoS_2 and Ti is accurately evaluated by 2D material thermionic emission current equation at flat-band gate voltage. The extracted contact resistance shows an obvious dependence on the drain current in four-terminal-measurements. In spite of a high Schottky barrier (0.3−0.35 eV), a small contact resistance ~1.3 $k\Omega\cdot\mu m$ can be achieved between monolayer MoS_2 and Ti, which is mainly due to the thinning of the Schottky barrier by the gate voltage. A record intrinsic mobility ~44 $cm^2/(V\cdot s)$ and record high ON-current (200 $\mu A/\mu m$ at V_{bg} = 30 V and V_{ds} = 8 V) in a monolayer back-gated MoS_2 FET on SiO_2 substrate have been observed at room temperature. In addition, the effective mobility of monolayer MoS_2 FET shows a clear drain voltage dependency, which is mainly from the

poor gate modulation as well as electron localization in MoS_2. In a back-gated monolayer MoS_2 FET with 90 nm SiO_2 back gate dielectric layer, velocity saturation is the main reason responsible for current saturation at relatively higher carrier density. Electron saturation velocity of monolayer MoS_2 is extracted to be $\sim 9.85 \times 10^5$ cm/s at V_{bg} = 30 V and V_{ds} = 6 V based on the electrical measurements. This work will provide useful guidance for the design of high performance monolayer MoS_2 FET for digital applications.

EXPERIMENTAL SECTION

Device Fabrication and Characterization. The source and drain regions are defined by electron-beam lithography followed by Ti metallization. Subsequently, 100 nm Au film is deposited on 10 nm Ti film by electron beam evaporation at 6×10^{-7} mbar. Heavily *n*-doped Si is used as the back gate. After metal lift-off, device is loaded into Lakeshore vacuum probe station. All measurements are performed in vacuum (1×10^{-6} mbar) at room temperature after annealing at 420 K for 12 h to remove any absorbed moisture and solvent molecules.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Gate modulation of top-gated monolayer FET with a thin high-K dielectric film, resistance extraction method, details of DFT calculations, derivation of thermionic-emission-current equation for 2D material, impact of current saturation on the performance of digital circuits, and carrier density of back-gated monolayer MoS_2 FET. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/nn506512j.

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